1. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a gate dielectric layer overlying said semiconductor substrate in each of said active areas;

depositing a metal layer overlying said gate dielectric layer;

implanting oxygen ions into said metal layer in said first active area to form an implanted metal layer and oxidizing said implanted metal layer to form a metal oxide layer; and

thereafter patterning said metal layer and said metal oxide layer to form a metal gate in said second active area and a metal oxide gate in said first active area wherein said PMOS area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

2. The method according to Claim 1 wherein said gate dielectric layer comprises one of the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

3. The method according to Claim 1 wherein said gate dielectric layer comprises one of the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

4. The method according to Claim 1 wherein said metal layer comprises one of the group containing ruthenium, iridium, osmium, rhodium, and rhenium.

5. The method according to Claim 1 wherein said oxygen ions are implanted at a dosage of between about 1 E 15 and 1 E 17 ions/cm^2 and an energy of between about 1 and 50 KeV.

6. The method according to Claim 1 wherein said step of oxidizing said implanted metal layer comprises annealing in an inert gas and wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

7. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a dummy gate in each of said active areas;

covering said dummy gates with a dielectric layer;

planarizing said dielectric layer whereby a top surface of each of said dummy gates is exposed;

removing said exposed dummy gates leaving gate openings to said semiconductor substrate;

forming a gate dielectric layer overlying said semiconductor substrate in each of said gate openings;

depositing a metal layer within said gate openings to form metal gates; and

implanting oxygen ions into said metal gate only in said first active area to form an implanted metal gate and oxidizing said implanted metal gate to form a metal oxide gate in said first area and a metal gate in said second active area wherein said PMOS area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of

an integrated circuit.

8. The method according to Claim 7 wherein said dummy gates comprise a first layer of silicon dioxide, a second layer of silicon nitride, and a third layer of polysilicon.

9. The method according to Claim 7 wherein said step of removing said dummy gates comprises one of the group containing: wet etching, dry etching, and a combination of wet and dry etching.

10. The method according to Claim 7 wherein said gate dielectric layer comprises one of the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

11. The method according to Claim 7 wherein said gate dielectric layer comprises one of the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

12. The method according to Claim 7 wherein said metal layer comprises one of the group containing ruthenium,

iridium, osmium, rhodium, and rhenium.

13. The method according to Claim 7 wherein said oxygen ions are implanted at a dosage of between about 1 E 15 and 1 E 17 ions/cm^2 and an energy of between about 1 and 50 KeV.

14. The method according to Claim 7 wherein said step of oxidizing said implanted metal layer comprises annealing in an inert gas or vacuum wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

15. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a gate dielectric layer overlying said semiconductor substrate in each of said active areas;

depositing a metal layer overlying said gate dielectric layer;

implanting first oxygen ions into said metal layer in said first active area to form an implanted metal

layer and oxidizing said implanted metal layer to form a first metal oxide layer;

implanting second oxygen ions into said metal layer in said second active area to form an implanted metal layer and oxidizing said implanted metal layer to form a second metal oxide layer wherein said first metal oxide layer has a different oxygen concentration from said second metal oxide layer; and

thereafter patterning said first and second metal oxide layers to form a first metal oxide gate in said first active area and a second metal oxide gate in said second active area wherein said PMOS active area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

16. The method according to Claim 15 wherein said gate dielectric layer comprises one of the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

17. The method according to Claim 15 wherein said gate dielectric layer comprises one of the group containing

zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

18. The method according to Claim 15 wherein said metal layer comprises one of the group containing ruthenium, iridium, osmium, rhodium, and rhenium.

19. The method according to Claim 15 wherein said first oxygen ions are implanted at a dosage of between about 1 E 15 and 1 E 16 ions/cm^2 and an energy of between about 1 and 50 KeV.

20. The method according to Claim 15 wherein said second oxygen ions are implanted at a dosage of between about 1 E 16 and 1 E 17 ions/cm^2 and an energy of between about 1 and 50 KeV.

21. The method according to Claim 15 wherein said steps of oxidizing said implanted metal layer comprises annealing in an inert gas wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

22. A method of forming dual-metal gate CMOS transistors in the fabrication of integrated circuits comprising:

providing a first and a second active area of a semiconductor substrate separated by isolation regions wherein one of said active areas will be a PMOS area and the other of said active areas will be an NMOS area;

forming a dummy gate in each of said active areas;

covering said dummy gates with a dielectric layer;

planarizing said dielectric layer whereby a top surface of each of said dummy gates is exposed;

removing said exposed dummy gates leaving gate openings to said semiconductor substrate;

forming a gate dielectric layer overlying said semiconductor substrate in each of said gate openings;

depositing a metal layer within said gate openings to form metal gates;

implanting first oxygen ions into said metal gate only in said first active area to form an implanted metal gate and oxidizing said implanted metal gate to form a first metal oxide gate in said first active area; and

implanting second oxygen ions into said metal gate only in said second active area to form an implanted metal gate and oxidizing said implanted metal gate to form a second metal oxide gate in said second active

area wherein said PMOS active area comprises one of said first and second active areas having a gate having a higher work function than said gate in the other of said active areas to complete formation said of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

23. The method according to Claim 22 wherein said dummy gates comprise a first layer of silicon dioxide, a second layer of silicon nitride, and a third layer of polysilicon.

24. The method according to Claim 22 wherein said step of removing said dummy gates comprises one of the group containing: wet etching, dry etching, and a combination of wet and dry etching.

25. The method according to Claim 22 wherein said gate dielectric layer comprises one of the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

26. The method according to Claim 22 wherein said gate dielectric layer comprises one of the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum

pentoxide, barium strontium titanates, and crystalline oxides.

27. The method according to Claim 22 wherein said metal layer comprises one of the group containing ruthenium, iridium, osmium, rhodium, and rhenium.

28. The method according to Claim 22 wherein said first oxygen ions are implanted at a dosage of between about 1 E 15 and 1 E 16 ions/cm^2 and an energy of between about 1 and 50 KeV.

29. The method according to Claim 22 wherein said second oxygen ions are implanted at a dosage of between about 1 E 16 and 1 E 17 ions/cm^2 and an energy of between about 1 and 50 KeV.

30. The method according to Claim 22 wherein said steps of oxidizing said implanted metal layer comprises one of the group of: annealing in an inert gas, annealing in an oxygen ambient, and plasma assisted oxidation and wherein said annealing is performed in one of the group of: a furnace process, a rapid thermal process, and a laser process.

31. A dual-metal gate CMOS integrated circuit device comprising:

an NMOS active area and a PMOS active area of a semiconductor substrate separated by isolation regions;

a metal gate in said NMOS active area over a gate dielectric layer; and

a metal oxide gate in said PMOS active area over a gate dielectric layer wherein said metal in said metal gate is the same material as said metal in said metal oxide gate and wherein said metal oxide gate has a higher work function than said metal gate.

32. The device according to Claim 31 wherein said gate dielectric layer comprises one of the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

33. The device according to Claim 31 wherein said gate dielectric layer comprises one of the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

34. The device according to Claim 31 wherein said metal layer comprises one of the group containing ruthenium,

iridium, osmium, rhodium, and rhenium.

35. A dual-metal gate CMOS integrated circuit device comprising:

an NMOS active area and a PMOS active area of a semiconductor substrate separated by isolation regions;

a metal gate in said PMOS active area over a gate dielectric layer; and

a metal oxide gate in said NMOS active area over a gate dielectric layer wherein said metal in said metal gate is the same material as said metal in said metal oxide gate and wherein said metal gate has a higher work function than said metal oxide gate.

36. The device according to Claim 35 wherein said gate dielectric layer comprises one of the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

37. The device according to Claim 35 wherein said gate dielectric layer comprises one of the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

38. The device according to Claim 35 wherein said metal layer comprises one of the group containing ruthenium, iridium, osmium, rhodium, and rhenium.

39. A dual-metal gate CMOS integrated circuit device comprising:

an NMOS active area and a PMOS active area of a semiconductor substrate separated by isolation regions;

a first metal oxide gate in said NMOS active area over a gate dielectric layer; and

a second metal oxide gate in said PMOS active area over a gate dielectric layer wherein said metal in said first metal oxide gate is the same material as said metal in said second metal oxide gate and wherein the concentration of said oxide in said first metal oxide gate is different from said the concentration of said oxide in said second metal oxide gate and wherein said second metal oxide gate has a higher work function than said first metal oxide gate.

40. The device according to Claim 39 wherein said gate dielectric layer comprises one of the group containing silicon dioxide, nitrided silicon dioxide, silicon nitride, and a combination thereof.

41. The device according to Claim 39 wherein said gate dielectric layer comprises one of the group containing zirconium oxide, hafnium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, and crystalline oxides.

42. The device according to Claim 39 wherein said metal layer comprises one of the group containing ruthenium, iridium, osmium, rhodium, and rhenium.